7. (Amended) A gateless electrostatic discharge (ESD) [ESD] protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region.

13. (Amended) An electrostatic discharge (ESD) [ESD] protection device comprising:

a substrate; and

an implant within the substrate, the implant including two implant regions spaced apart by only the substrate region, wherein the substrate comprises a first conductivity type and the two implant regions comprise a second conductivity type, wherein conductivity between the two implant regions is not controlled by voltage potential of a gate above the two implant regions.

17. (Amended) An integrated circuit comprising:

a voltage source;

an external bonding pad; and

an electrostatic discharge (ESD) [ESD] protection device connected between the bonding pad and the voltage source, the

ESD protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

23. (Amended) An integrated circuit comprising:

a first voltage source;

a second voltage source;

an external bonding pad;

a first electrostatic discharge (ESD) [ESD] protection device connected between the first voltage source and the external bonding pad; and

a second ESD protection device connected between the second voltage source and the external bonding pad, wherein the second ESD protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

27. (Amended) An integrated circuit comprising:

a voltage source;

an external bonding pad;

an internal circuit connected to the external bonding pad at a node; and

an electrostatic discharge (ESD) [ESD] protection device connected between the node and the voltage source, the ESD protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

28. (Amended) An integrated circuit comprising:

a first voltage source;

a second voltage source;

an external bonding pad;

an internal circuit connected to the external bonding pad at a node;

a first electrostatic discharge (ESD) [ESD] protection device connected between the first voltage source and the node;

and

a second ESD protection device connected between the second voltage source and the node, wherein the second ESD protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

29. (Amended) A semiconductor chip comprising:

a package having a plurality of pins; and

an electrostatic discharge (ESD) [ESD] protection device connected to at least one of the pins, the protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions.

33. (New) A chip comprising:

a package having a plurality of pins; and

a protection device connected to at least one of the pins, the protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped

region by only the substrate region.

34. (New) A chip comprising:

a package having a plurality of pins; and

a protection device connected to at least one of the pins, the protection device comprising:

a substrate; and

an implant within the substrate, the implant including two implant regions spaced apart by only the substrate region, wherein the substrate comprises a first conductivity type and the two implant regions comprise a second conductivity type, wherein conductivity between the two implant regions is not controlled by voltage potential of a gate above the two implant regions.

35. (New) A chip comprising:

a package having a plurality of pins; and

a protection device connected to at least one of the pins, the protection device comprising:

a substrate;

a first doped region formed in the substrate; and

a second doped region formed in the substrate and separated from the first doped region by only the substrate region such that an amount current flowing between the first and second doped regions is not controlled by a voltage potential of a gate above the first and second doped regions.